What is claimed is:

1. A MOSFET on a semiconductor substrate, said MOSFET including a gate electrode and having a recessed channel in said semiconductor substrate, said recessed channel being defined by a recessed trench, in which the critical dimension of said recessed trench is greater than the critical dimension of said gate electrode such that the gate electrode is overlapped by the recessed trench.

2. The MOSFET of claim 1, wherein said recessed trench has a round profile.

3. A MOSFET having a recessed channel defined by a trench formed in a semiconductor substrate, said MOSFET comprising:

a gate electrode, which includes a gate oxide layer on an inner wall of said recessed trench, a gate conductive layer which fills the recessed trench and rises over the semiconductor substrate, wherein a portion of the gate conductive layer rising over the semiconductor substrate is smaller than the critical dimension of the recessed trench, and a capping layer formed on the gate conductive layer has the same critical dimension as the gate conductive layer;

spacers surrounding sidewalls of the gate electrode; and

a source/drain region which is formed in the semiconductor substrate on both sides of the gate electrode so as to be insulated from the gate conductive layer by the gate oxide layer.

4. The MOSFET of claim 3, wherein the recessed trench has round profile.

5. The MOSFET of claim 3, wherein the gate oxide layer is selected from the group consisting of a silicon oxide layer, a titanium oxide layer, and a tantalum oxide layer.

6. The MOSFET of claim 3, wherein the gate conductive layer comprises a conductive polysilicon layer that completely fills the recessed trench and a metal layer formed on the conductive polysilicon layer.

7. The MOSFET of claim 3, wherein the spacers are extended into the semiconductor substrate to a depth of 500 Å or less.

8. A method of forming a MOSFET having a recessed channel, comprising:

forming a recessed trench;

forming a gate oxide layer on an inner wall of said recessed trench;

sequentially forming a gate conductive layer and a capping layer on the gate oxide layer so as to completely fill the recessed trench;

forming a gate electrode that is overlapped by the gate conductive layer filling the recessed trench by patterning the capping layer and the gate conductive layer which rises over the semiconductor substrate to have a smaller critical dimension than that of the recessed trench; and

forming a source/drain region by implanting impurity ions into the semiconductor substrate on both sides of the gate electrode.

9. The method of claim 8, wherein forming the recessed trench comprises:

forming a rectangular trench in the semiconductor substrate using a reactive ion beam etch process; and

making the recessed trench have a round profile by further etching the trench using a chemical dry etch process.

10. The method of claim 9, wherein the rectangular trench is formed to a depth of about 1000 Å to 1500 Å and is further etched by about 100 Å to 200 Å using a chemical dry etch process.

11. The method of claim 8, wherein the gate oxide layer is formed from the group consisting of: a silicon oxide layer, a titanium oxide layer, and a tantalum oxide layer.

12. The method of claim 8, wherein the gate conductive layer comprises a conductive polysilicon layer that completely fills the recessed trench and a metal layer formed on the conductive polysilicon layer.

13. The method of claim 8, wherein forming the recessed trench further compromises:

forming a sacrificial oxide layer by thermally oxidizing the semiconductor substrate; and

removing the sacrificial oxide layer using a wet etch process.

14. The method of claim 8, wherein forming the gate electrode comprises recessing the gate conductive layer that fills the recessed trench to a depth of 500 Å or less from the surface of the semiconductor substrate by adjusting the etching time.

15. The method of claim 8, further comprising forming spacers on the sidewalls of the gate electrode.

16. A MOSFET having a gate electrode formed on a semiconductor substrate by a photolithographic process and a recessed channel defined by a recessed trench in said semiconductor substrate, wherein the critical dimension of said recessed trench is greater than the critical dimension of said gate electrode whereby the misalignment margin for said photolithographic process used to form said gate electrodes can be increased, and both overlap capacitance and gate induced drain leakage (GIDL) are reduced.